



IFW

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of)	
)	
Lane, et al.)	For: METHOD FOR ACCOMODATING
)	SMALL MINIMUM DIE IN
)	BONDED AREA ARRAY
)	PACKAGES
Serial No. 10/830,188)	
)	
Filed: April 21, 2004)	Group No. 2822

REQUEST FOR CORRECTION OF OFFICIAL FILING RECEIPT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: OFFICE OF INITIAL PATENT EXAMINATION'S CUSTOMER SERVICE CENTER

Dear Sir:

Upon review of the Filing Receipt, an error in the "Domestic Priority data as claimed by applicant" as listed thereon was noted. Applicants request that this error be corrected and that a new Official Filing Receipt be issued.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on:

July 7, 2005

(Date of Deposit)

Theresa Badet

(Name of the Person Making Deposit)

Theresa Badet
(Signature)

The Domestic Priority data as claimed by applicant states this application is a continuation, however, this application is a divisional.

Enclosed herewith is a copy of the front page of the patent application indicating the subject application is a divisional of 10/624,787 filed July 21, 2003 which claims priority to U.S. Provisional Application No. 60/399,091 filed July 26, 2002.

Also enclosed, for your convenience, is a copy of the incorrect Official Filing Receipt showing that the Domestic priority data has been incorrectly entered as "CON (continuation)".

Applicants submit that the above-indicated error is an error made on the part of the Applicant. Please charge Deposit Account No. 17-0026 in the name of QUALCOMM, Incorporated \$130.00 for the filing of the Petition to Correct the Filing Receipt. The Commissioner is also hereby authorized to charge any additional fees or credit any overpayment to Deposit Account No. 17-0026. Applicant respectfully requests that the noted error in the "Domestic Priority data" be corrected and a new Official Filing Receipt be issued to Applicants.

Respectfully submitted,

Dated: July 7, 2005

By: 

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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/830,188	04/21/2004	2822	770	020378D1	10	15	3

CONFIRMATION NO. 7730

23696

Qualcomm Incorporated
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FILING RECEIPT



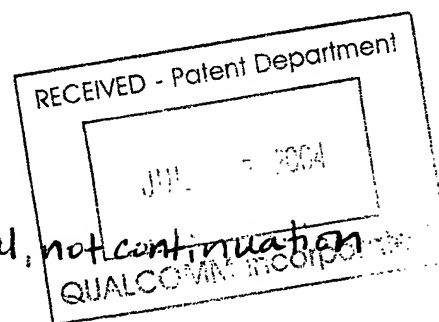
OC000000013099069

Date Mailed: 06/30/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

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 Tom Gregorich, San Diego, CA;



Domestic Priority data as claimed by applicant

This application is a ^{81V} continuation of 10/624,787 07/21/2003
 which claims benefit of 60/399,091 07/26/2002

divisional, not continuation

Foreign Applications

If Required, Foreign Filing License Granted: 06/28/2004

Projected Publication Date: 10/07/2004

Non-Publication Request: No

Early Publication Request: No

Title

Method for accommodating small minimum die in wire bonded area array packages

Preliminary Class

257

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**

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METHOD FOR ACCOMMODATING SMALL MINIMUM DIE IN WIRE BONDED AREA ARRAY PACKAGES

BACKGROUND OF THE DISCLOSURE

Related Applications

[0001] This application is a divisional application of Application No. 10/624,787; filed on July 21, 2003 (Docket No. 020378) which claims priority to U.S. Provisional Application No. 60/399,091. filed on July 26, 2002.

Field of the Disclosure

[0002] This disclosure relates generally to microchip packaging. More specifically, the present disclosure relates to a method of accommodating small minimum die in wire bonded area array packages.

Brief Description of the Related Art

[0003] Integrated circuit (IC) packages, particularly area array packages such as ball grid arrays (BGA) and land grid arrays (LGA), often contain sophisticated electrical subsystems to connect the many components of a die to a device or circuit board. Over the years, package designers have struggled to keep pace with a modern trend toward higher pin counts brought about by higher integration of feature sets. At the same time, dice have continued to shrink in physical size due in part to significant improvements in wafer processing technology. Complex digital signal processor (DSP), for instance, commonly contain several hundred electrical leads. In an effort to keep pace with these improvements, fundamental changes are needed in the way chips are packaged.

[0004] Package designers have tried to accommodate diminishing die size and growing pin counts in a number of ways. One technique involves miniaturizing the physical size of each bond finger. But there is a lower limit to the size of a bond finger—the smallest bond wire is around 0.7 mils in diameter, and a reduced wire diameter also reduces the maximum wire length available. A bond finger must at least be wide enough to accommodate a wire bond. Thus, it is often impractical to further shrink the bond fingers.

[0005] Other approaches for accommodating a large pin-count die include rearranging the package's bond finger array to form two or more rows of bond fingers, or forming a